

Mr. Jayant Kumar Rout



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Joining in the Institute : 30.04.2007

Teaching (UG/PG) : VLSI Design

Area of specialization : VLSI

Experience : 31.01.2005 to 29.04.2007 at CEB
30.04.2007 to till date in ITER

Training attended : Attended a training course during 2001 summer
vacation in the Kalinga Software Private Limited,
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